IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	William N. Joy, Marc Tremblay, Gary Lauterbach and Joseph I. Chamdani		
Title:	SWITCHING METHOD IN A MULTI-THREADED PROCESSOR		
Application No.:	Not yet assigned	Filed:	Herewith
Examiner:	Not yet assigned	Group Art Unit:	Not yet assigned
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COMMISSIONER FOR PATENTS
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PRELIMINARY AMENDMENT

Prior to the first action on the merits, please amend the above-identified application as follows:

In the Specification

On page 1, on the first line of the specification, insert the following cross-reference information:

CROSS-REFERENCE

This application is a continuation of Application No. 10/074,419, filed February 12, 2002, which is itself a divisional of Application No. 09/309,735, filed May 11, 1999, now U.S. Patent No. 6,507,862. Application Nos. 10/074,419 and 09/309,735 are each incorporated, by reference herein, in their entirety.

The present application is related to subject matter disclosed in the following patent applications:

1. United States Patent Application No. 09/309,732 entitled "Processor With Multiple-Thread, Vertically-Threaded Pipeline" naming William Joy, Marc Tremblay, Gary Lauterbach and Joseph Chamdani as inventors and filed on May 11, 1999.

2. United States Patent Application No. 09/309,731, now U.S. Patent No. 6,351,808, entitled "Vertically-Threaded Processor with Multi-Dimensional Storage" naming William Joy, Marc Tremblay, Gary Lauterbach and Joseph Chamdani as inventors and filed on May 11, 1999.

3. United States Patent Application No. 09/309,730 entitled "Vertically-Threaded Processor By Multiple-Bit Flip-Flop Global Substitution" naming William Joy, Marc Tremblay, Gary Lauterbach and Joseph Chamdani as inventors and filed on May 11, 1999.

4. United States Patent Application No. 09/309,734 entitled "Multiple-Thread Processor with Single-Thread Interface Shared Among Threads" naming William Joy, Marc Tremblay, Gary Lauterbach and Joseph Chamdani as inventors and filed on May 11, 1999.

5. United States Patent Application No. 09/309,733, now U.S. Patent No. 6,341,347, entitled "Thread Switch Logic in a Multiple-Thread Processor" naming William Joy, Marc Tremblay, Gary Lauterbach and Joseph Chamdani as inventors and filed on May 11, 1999.

Please replace the paragraph on page 8, beginning at line 12, with the following paragraph:

FIGURES ~~16~~ **16A and 16B** are a schematic circuit diagram illustrates a suitable bit storage circuit storing one bit of the local registers file for the multi-dimensional register file with eight windows.

Please replace the paragraph on page 8, beginning at line 17, with the following paragraph:

FIGURES ~~18 is~~ **18A, 18B, 18C and 18D** are a schematic circuit diagram illustrating an implementation of a multi-dimensional register file for registers shared across a plurality of windows.

Replace the paragraph beginning on page 34, line 18 through page 35, line 7 with the following:

The external cache control unit **1022** is also connected to a peripheral component interconnect (PCI) bus **1032** via a PCI controller **1030**. The external cache control unit **1022** is further connected to a Dynamic Random Access Memory (DRAM) **1034** and an UltraPort Architecture Interconnect (UPA) bus **1026** via a memory control unit (MCU) **1028**. The external cache control unit **1022** and the memory control unit (MCU) **1028** are unified between thread 0 and thread 1 to perform functions of cache miss processing and interfacing with external devices to supply, in combination, a plurality of execution threads to the thread 0 machine state block **1010** and the thread 1 machine state block **1012**. The unified external cache control unit **1022** and memory control unit (MCU) **1028** include thread identifier (TID) tagging to specify and identify the thread that is accessed via the L2 cache SRAM **1024**, the PCI bus **1032**, the DRAM **1034**, and the UPA bus **1026**. The PCI controller **1030** and the MCU **1028** are shared between threads using a single port identifier. Thread ID tagging is implemented in processor components that are non-stalling including, for example, a carry (logN)-bit TID in L1 and L2 caches (both data and instruction caches), translation look-aside buffers (TLBs), asynchronous interfaces of load buffers, an external memory management unit (MMU) interface, and the like. In non-stalling components, only a single thread passes through the component at one time so that no stalled state exists that would be stored. The thread ID bits identify which thread is active in the component.